FIG. 1

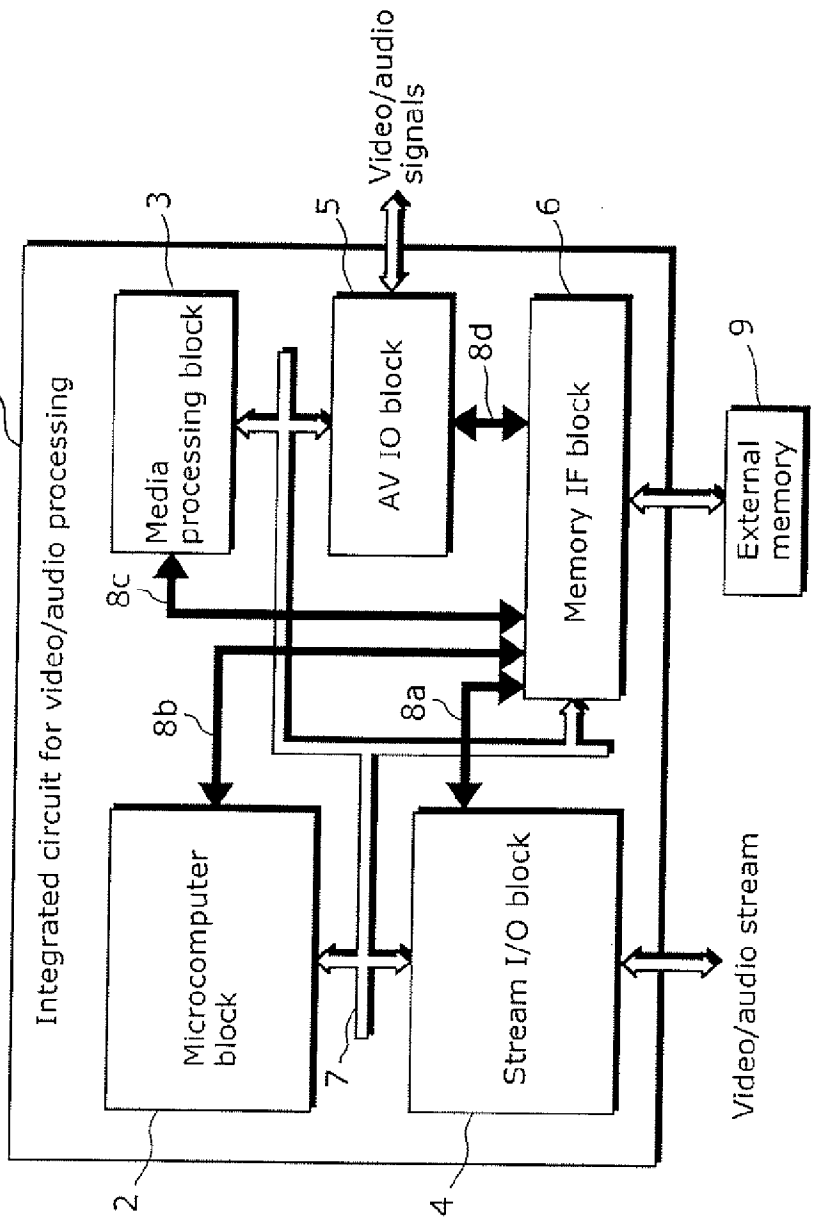

1
Integrated circuit for video/audio processing
2
Microcomputer block
3
Media processing block
4
Stream I/O block
5
AV IO block
6
Memory IF block
7
8a
8b
8c
8d
9
External memory
Video/audio signals
Video/audio stream

FIG. 2

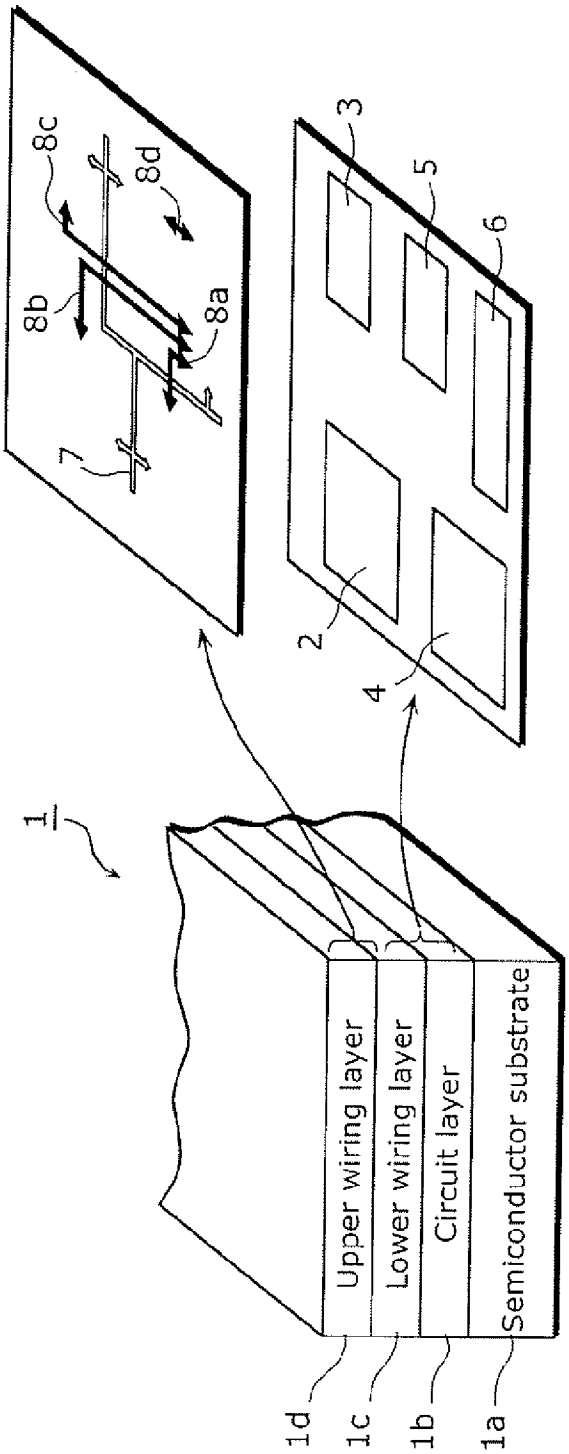

1
Upper wiring layer
Lower wiring layer
Circuit layer
Semiconductor substrate
1d
1c
1b
1a
2
3
4
5
6
7
8a
8b
8c
8d

FIG. 3

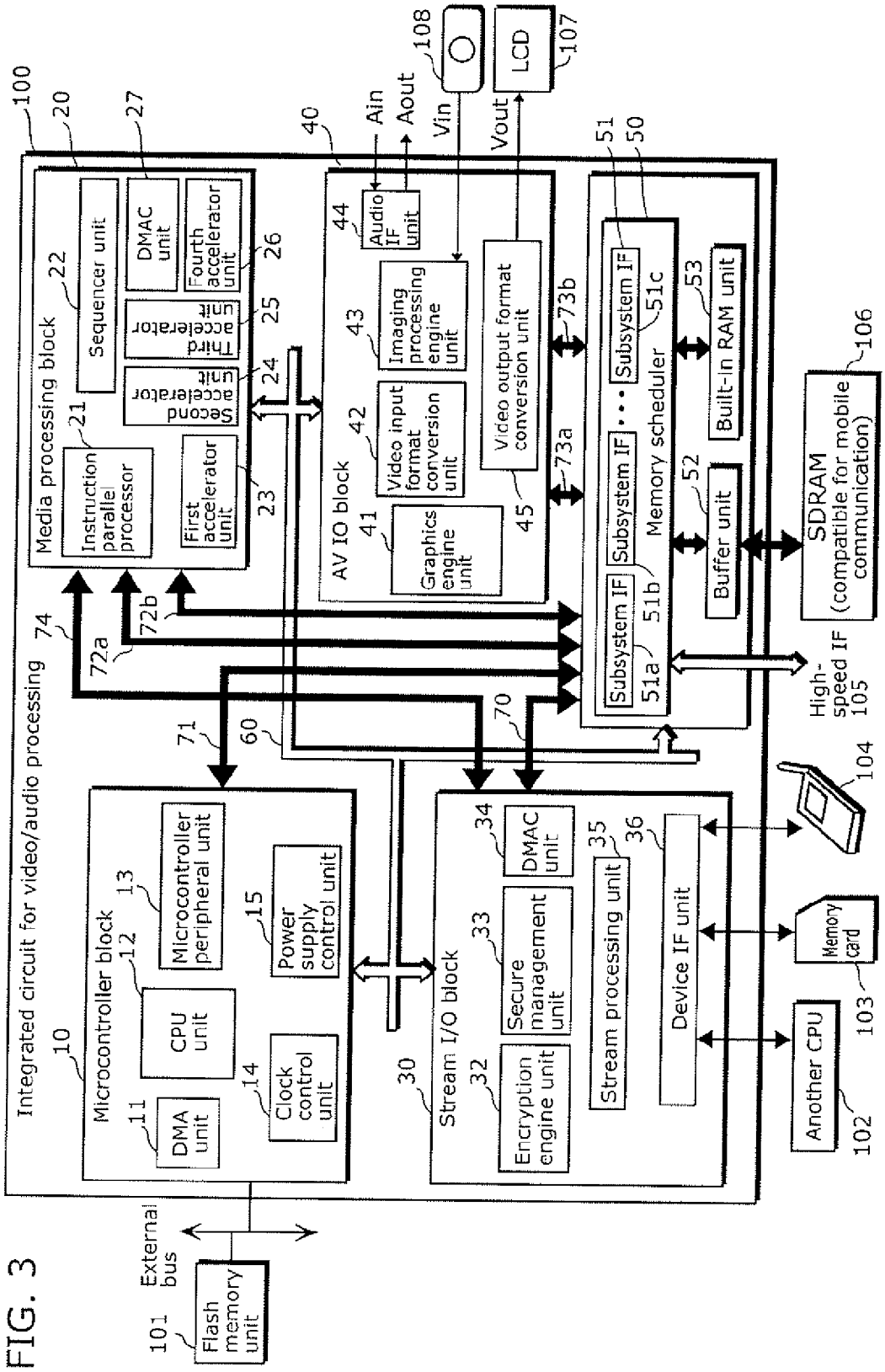

100
Integrated circuit for video/audio processing
Media processing block
20
Instruction parallel processor
21
Sequencer unit
22
First accelerator unit
23
Second accelerator unit
24
Third accelerator unit
25
Fourth accelerator unit
26
DMAC unit
27
AV IO block
40
Graphics engine unit
41
Video input format conversion unit
42
Imaging processing engine unit
43
Audio IF unit
44
Video output format conversion unit
45
Microcontroller block
10
DMA unit
11
CPU unit
12
Microcontroller peripheral unit
13
Clock control unit
14
Power supply control unit
15
Stream I/O block
30
Encryption engine unit
32
Secure management unit
33
DMAC unit
34
Stream processing unit
35
Device IF unit
36
Memory scheduler
50
Subsystem IF
51
Subsystem IF
51a
Subsystem IF
51b
Subsystem IF
51c
Buffer unit
52
Built-in RAM unit
53
SDRAM (compatible for mobile communication)
106
High-speed IF
105
Ain
Aout
Vin
Vout
108
LCD
107
74
72a
72b
71
60
70
73a
73b
External bus
Flash memory unit
101
Another CPU
102
103
Memory card
104

FIG. 4

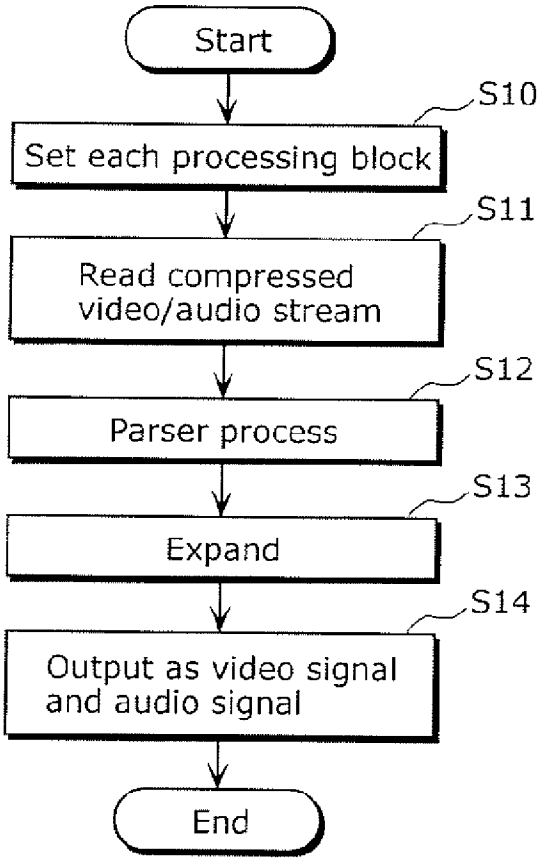
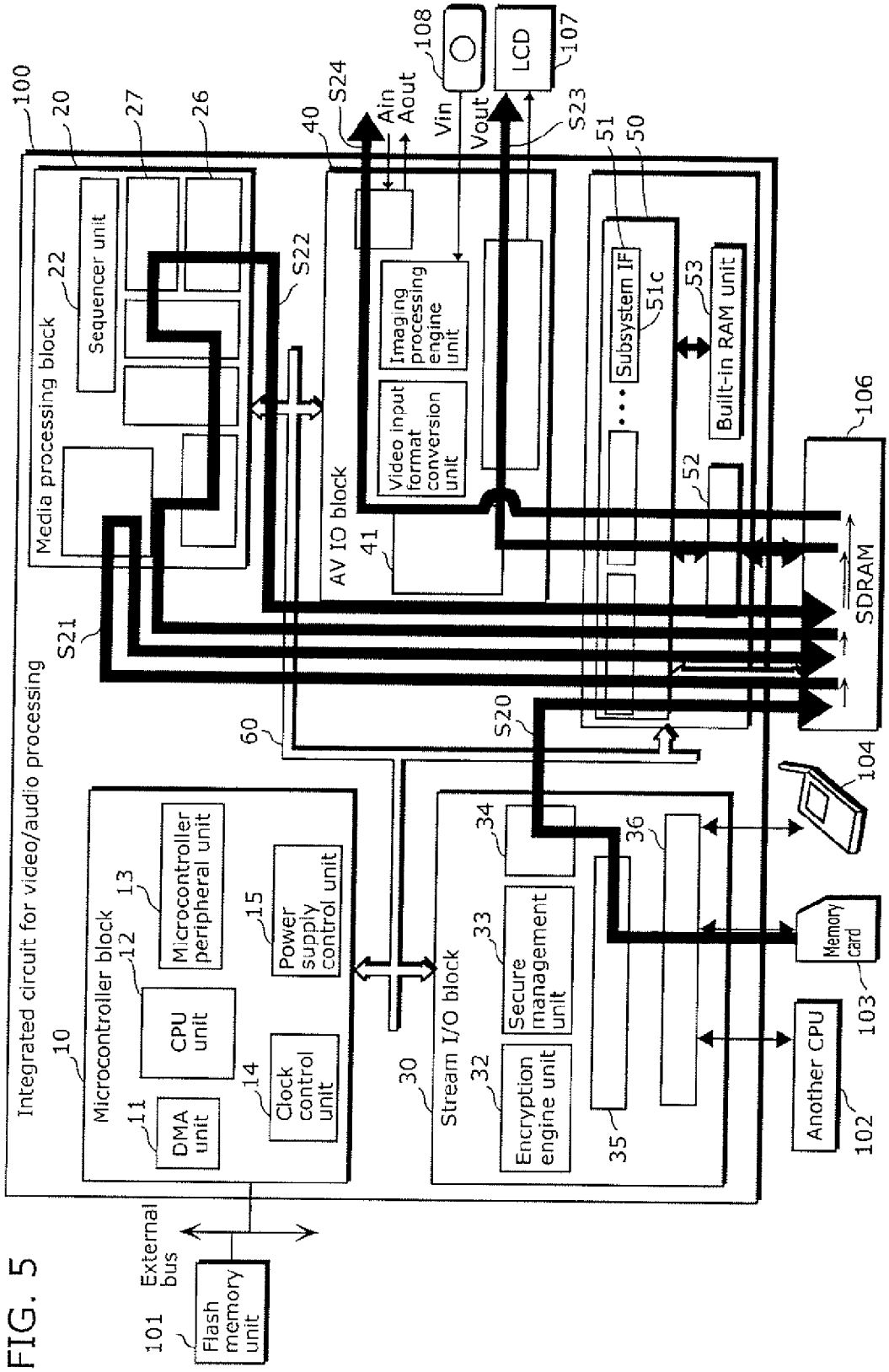

Start
S10
Set each processing block
S11
Read compressed video/audio stream
S12
Parser process
S13
Expand
S14
Output as video signal and audio signal
End

FIG. 5


100
Integrated circuit for video/audio processing
10
Microcontroller block
11
DMA unit
12
CPU unit
13
Microcontroller peripheral unit
14
Clock control unit
15
Power supply control unit
20
Media processing block
22
Sequencer unit
26
27
S21
S22
40
AV IO block
41
Video input format conversion unit
Imaging processing engine unit
S24
Ain
Aout
Vin
Vout
108
LCD
107
S23
51
50
Subsystem IF
51c
53
Built-in RAM unit
52
106
SDRAM
60
S20
30
Stream I/O block
32
Encryption engine unit
33
Secure management unit
34
35
36
104
Memory card
103
Another CPU
102
External bus
101
Flash memory unit

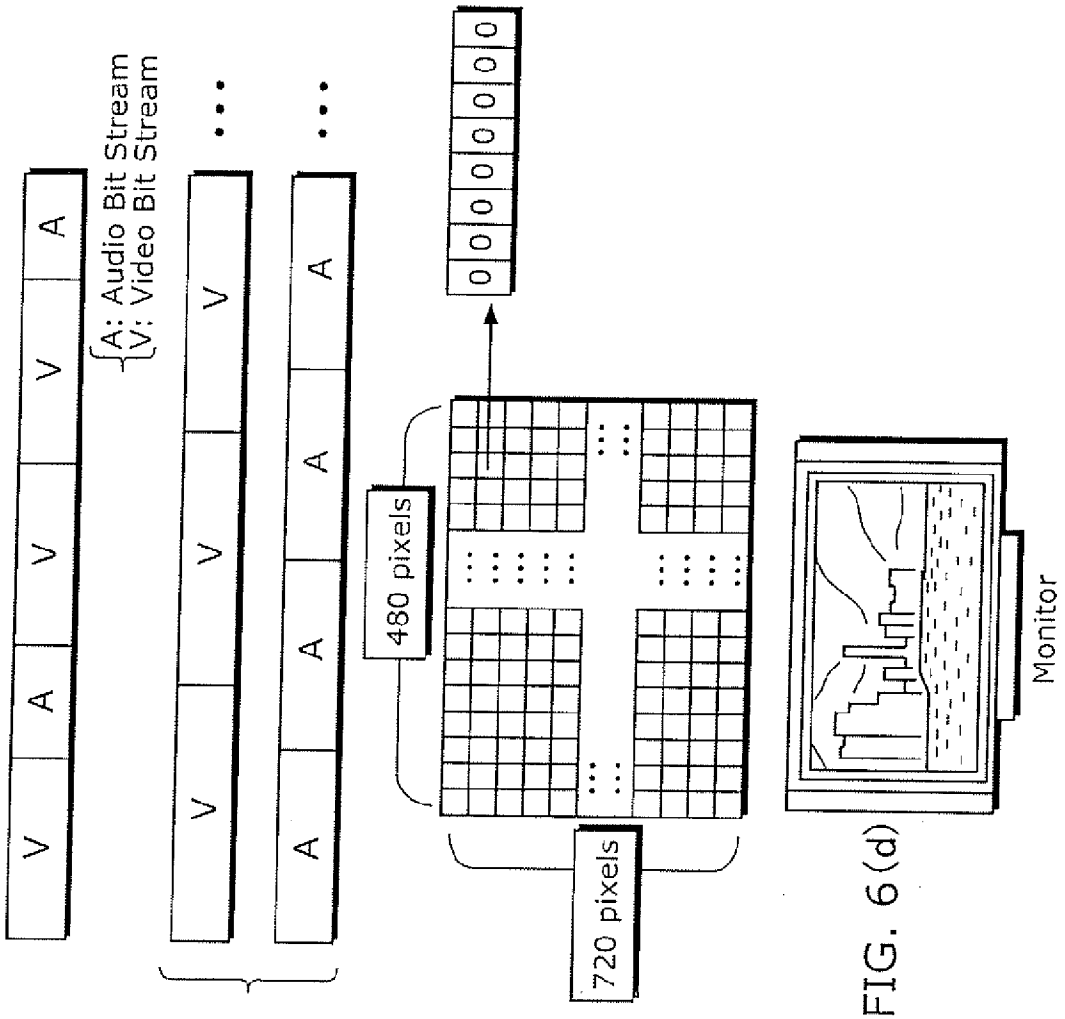


FIG. 6(a)

FIG. 6(b)

FIG. 6(c)

FIG. 6(d)

FIG. 7

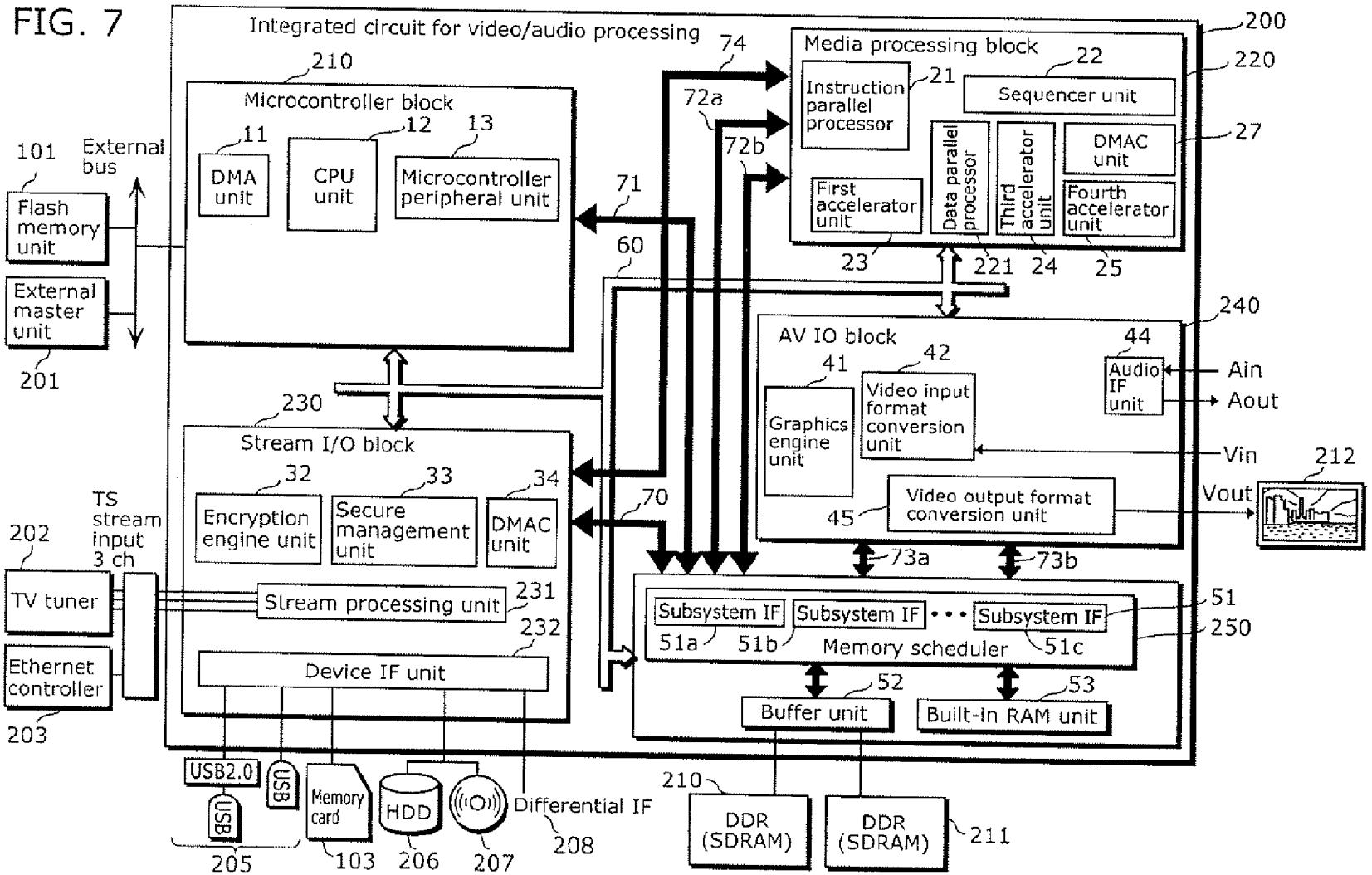

Integrated circuit for video/audio processing
200
Media processing block
220
Instruction parallel processor
21
Sequencer unit
22
DMAC unit
27
First accelerator unit
23
Data parallel processor
221
Third accelerator unit
24
Fourth accelerator unit
25
74
72a
72b
71
60
Microcontroller block
210
DMA unit
11
CPU unit
12
Microcontroller peripheral unit
13
101
External bus
Flash memory unit
External master unit
201
240
AV IO block
41
Graphics engine unit
42
Video input format conversion unit
44
Audio IF unit
Ain
Aout
Vin
212
Vout
45
Video output format conversion unit
230
Stream I/O block
32
Encryption engine unit
33
Secure management unit
34
DMAC unit
70
202
TS stream input 3 ch
TV tuner
Ethernet controller
203
Stream processing unit
231
232
Device IF unit
73a
73b
Subsystem IF
Subsystem IF
Subsystem IF
51
51a
51b
51c
Memory scheduler
250
52
Buffer unit
53
Built-in RAM unit
USB2.0
USB
USB
205
Memory card
103
HDD
206
207
Differential IF
208
210
DDR (SDRAM)
DDR (SDRAM)
211

FIG. 8

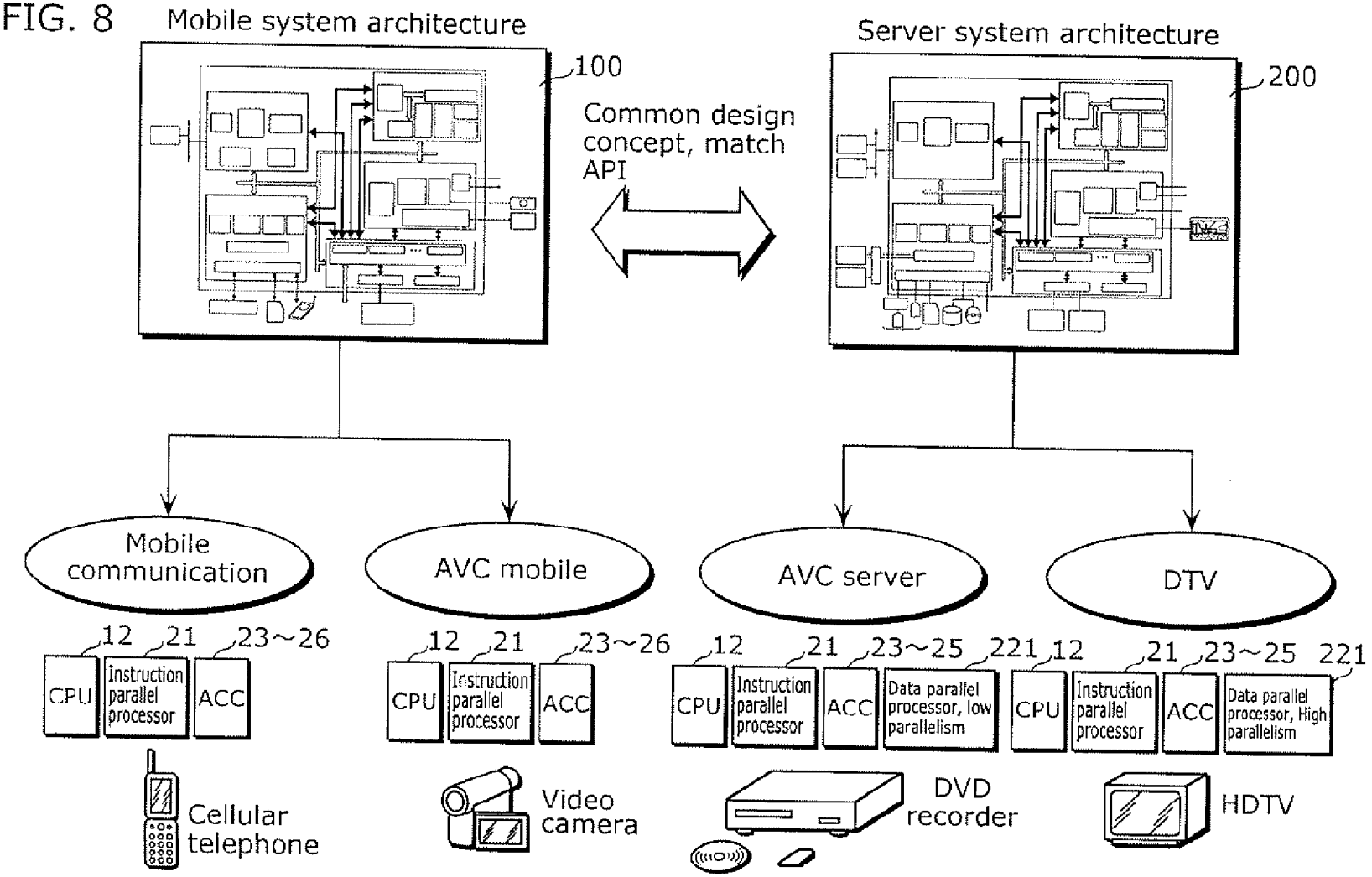

Mobile system architecture
100
Common design concept, match API
Server system architecture
200
Mobile communication
AVC mobile
AVC server
DTV
12
21
23~26
CPU
Instruction parallel processor
ACC
Cellular telephone
Video camera
23~25
221
Data parallel processor, low parallelism
DVD recorder
Data parallel processor, High parallelism
HDTV

FIG. 9

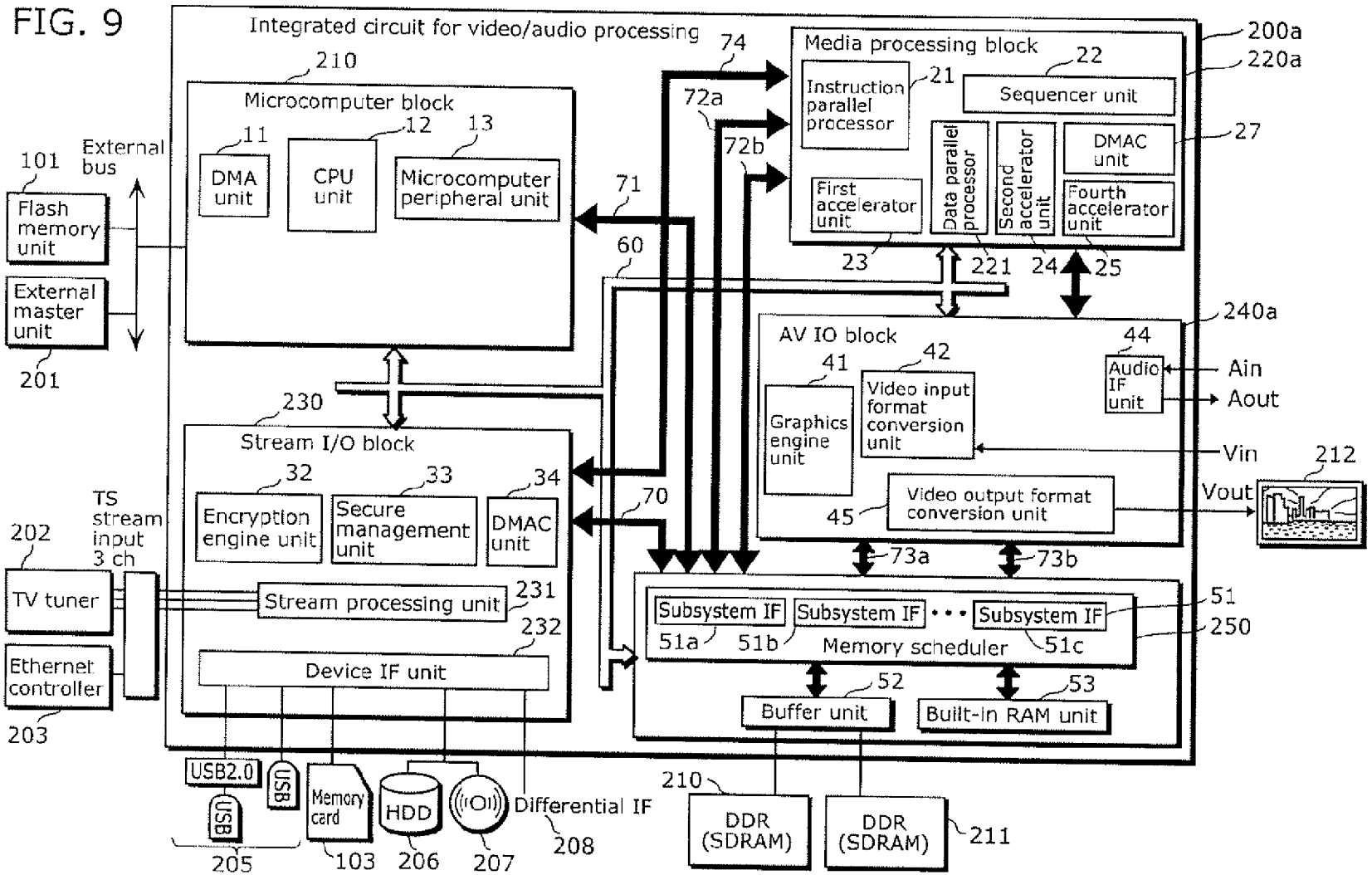

Integrated circuit for video/audio processing
200a
220a
Media processing block
Instruction parallel processor
21
Sequencer unit
22
DMAC unit
27
First accelerator unit
Data parallel processor
Second accelerator unit
Fourth accelerator unit
23
221
24
25
74
72a
72b
71
60
210
Microcomputer block
DMA unit
11
CPU unit
12
Microcomputer peripheral unit
13
101
External bus
Flash memory unit
External master unit
201
240a
AV IO block
41
Graphics engine unit
42
Video input format conversion unit
44
Audio IF unit
Ain
Aout
Vin
212
Vout
45
Video output format conversion unit
230
Stream I/O block
32
Encryption engine unit
33
Secure management unit
34
DMAC unit
70
TS stream input 3 ch
202
TV tuner
Ethernet controller
203
Stream processing unit
231
232
Device IF unit
73a
73b
Subsystem IF
Subsystem IF
Subsystem IF
51
250
51a
51b
Memory scheduler
51c
52
Buffer unit
53
Built-in RAM unit
USB2.0
USB
USB
205
Memory card
103
HDD
206
207
Differential IF
208
210
DDR (SDRAM)
DDR (SDRAM)
211

FIG. 10

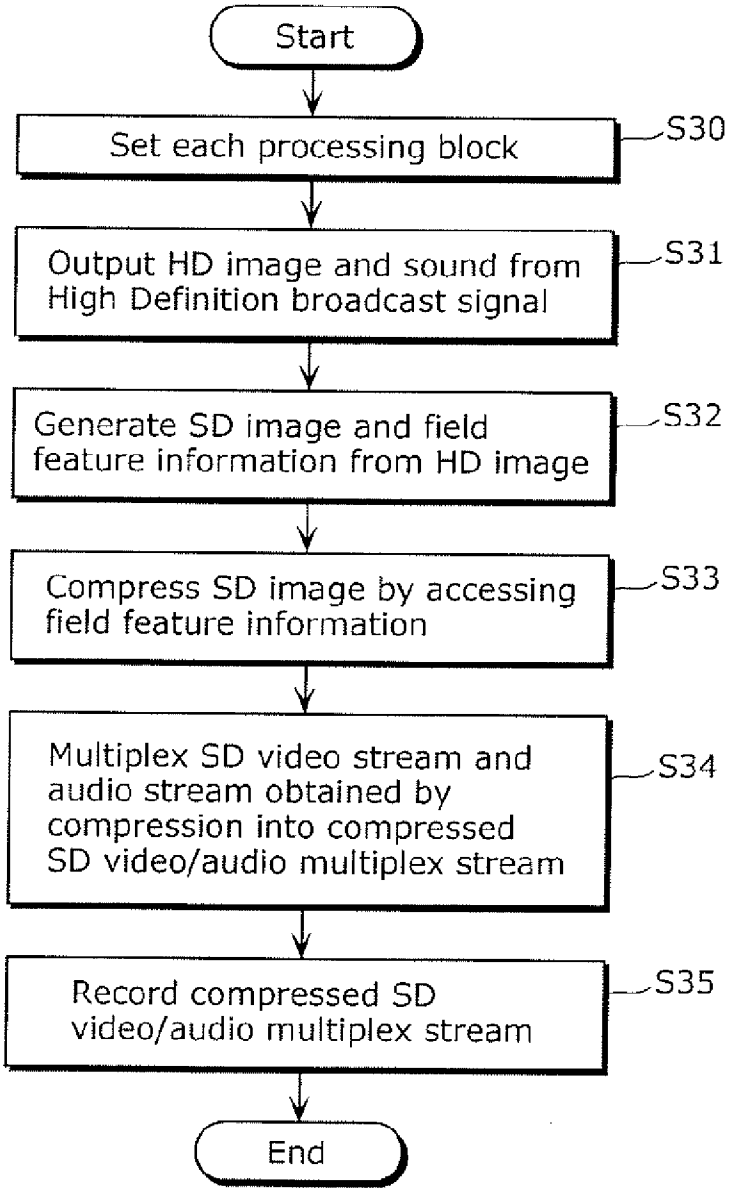
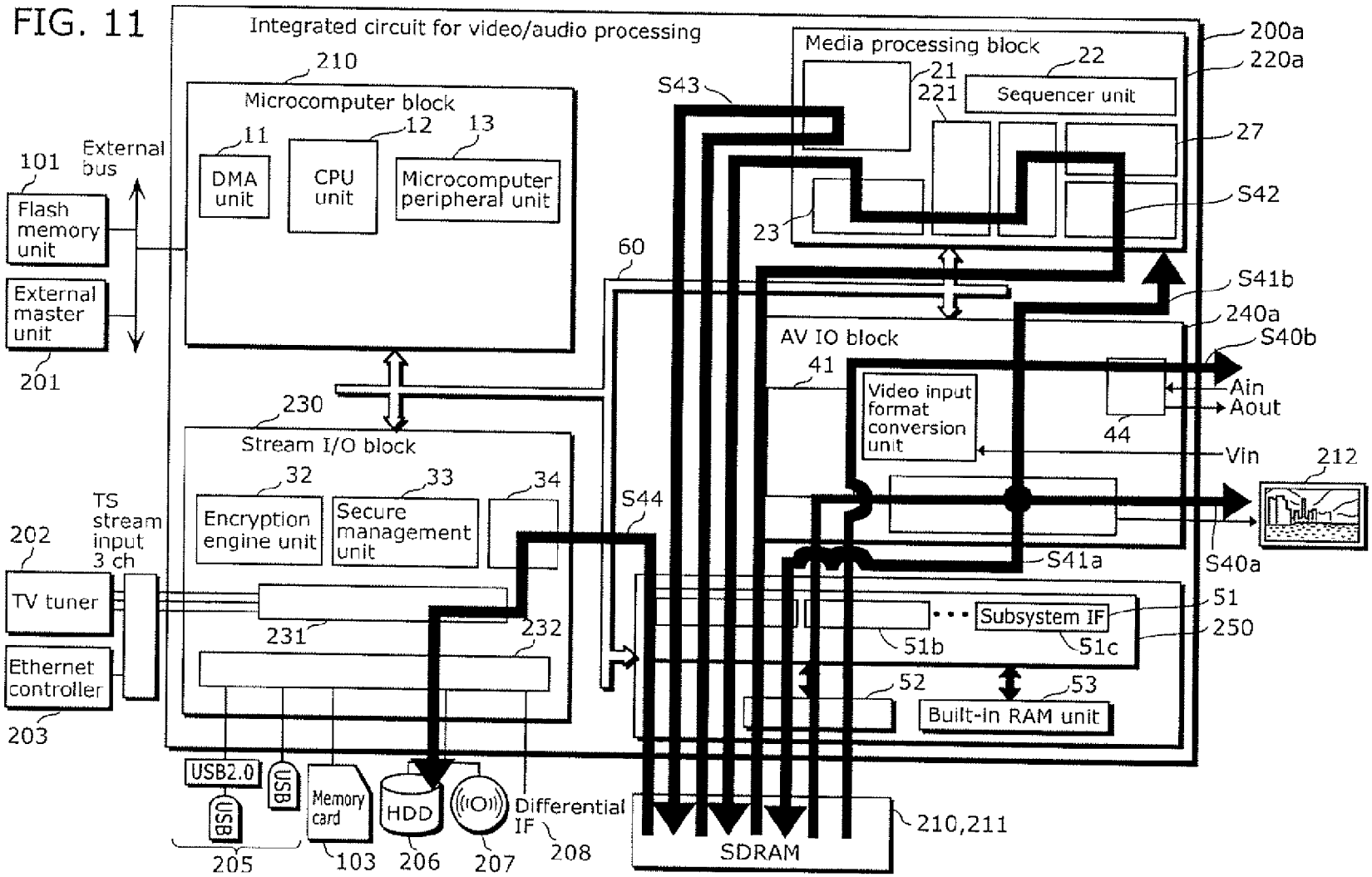

Start
Set each processing block
S30
Output HD image and sound from High Definition broadcast signal
S31
Generate SD image and field feature information from HD image
S32
Compress SD image by accessing field feature information
S33
Multiplex SD video stream and audio stream obtained by compression into compressed SD video/audio multiplex stream
S34
Record compressed SD video/audio multiplex stream
S35
End

FIG. 11


Integrated circuit for video/audio processing
200a
220a
Media processing block
21
221
22
Sequencer unit
27
S43
S42
23
210
Microcomputer block
11
DMA unit
12
CPU unit
13
Microcomputer peripheral unit
60
S41b
240a
AV IO block
S40b
41
Video input format conversion unit
44
Ain
Aout
Vin
212
230
Stream I/O block
32
Encryption engine unit
33
Secure management unit
34
S44
S41a
S40a
51
Subsystem IF
51c
51b
250
231
232
52
53
Built-in RAM unit
101
External bus
Flash memory unit
External master unit
201
202
TS stream input 3 ch
TV tuner
Ethernet controller
203
USB2.0
USB
USB
Memory card
HDD
Differential IF
205
103
206
207
208
SDRAM
210,211

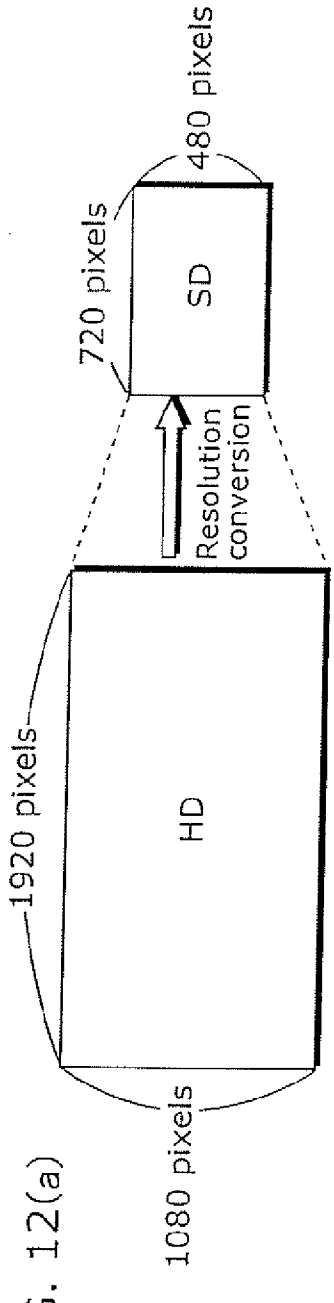


FIG. 12(a)

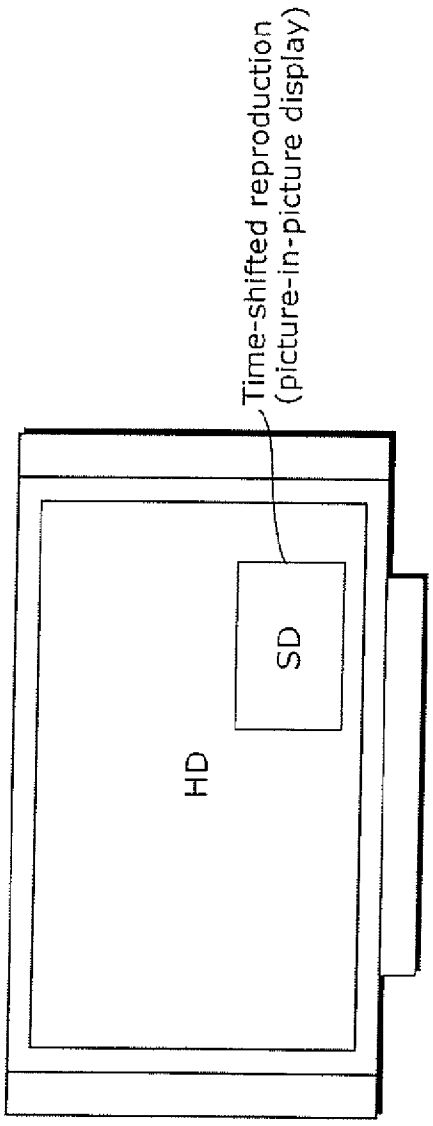


FIG. 12(b)

FIG. 13

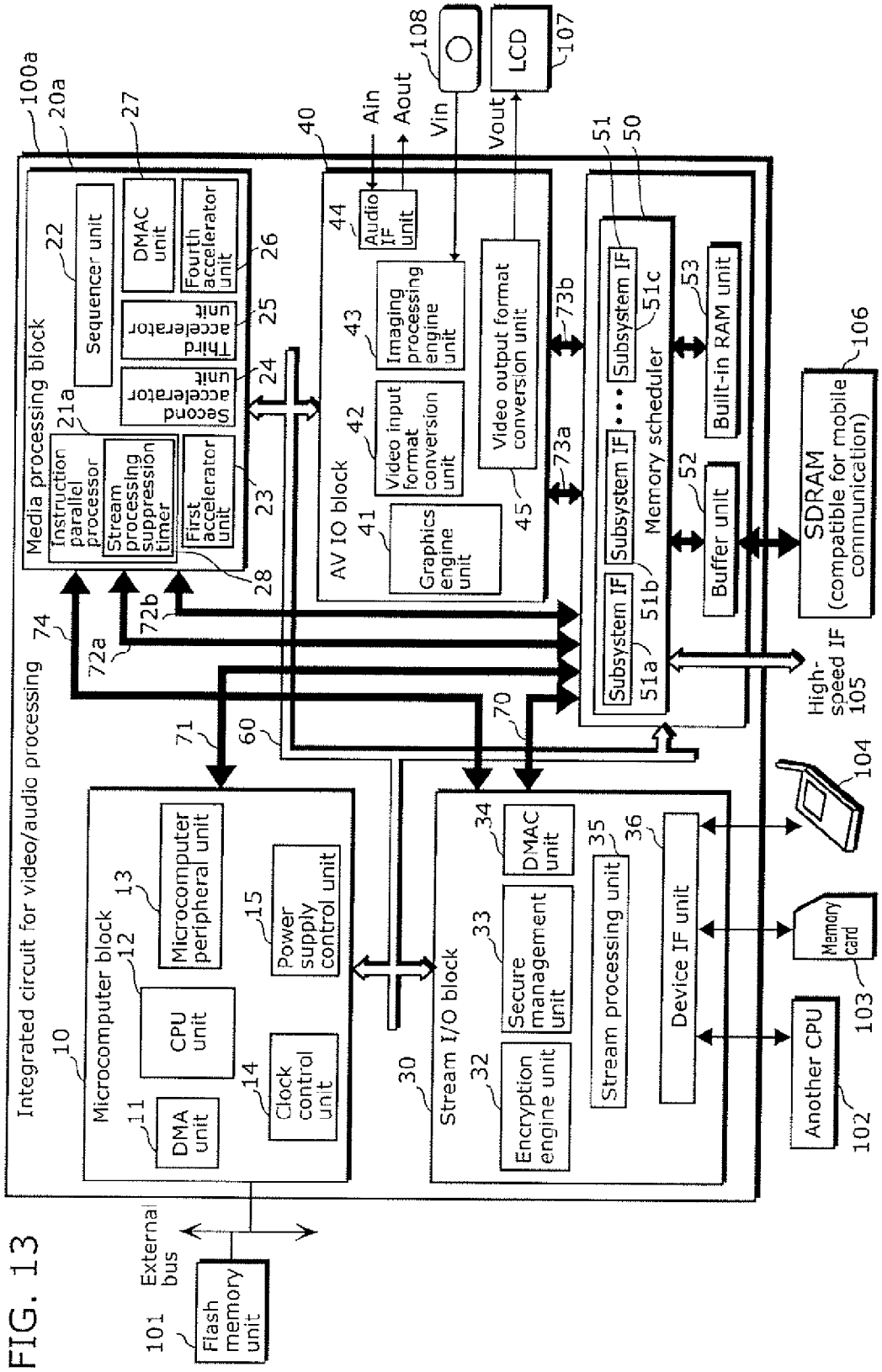

Integrated circuit for video/audio processing
100a
20a
Media processing block
Instruction parallel processor
Stream processing suppression timer
First accelerator unit
Second accelerator unit
Third accelerator unit
Fourth accelerator unit
Sequencer unit
DMAC unit
21a
22
23
24
25
26
27
28
Microcomputer block
DMA unit
CPU unit
Microcomputer peripheral unit
Clock control unit
Power supply control unit
10
11
12
13
14
15
Stream I/O block
Encryption engine unit
Secure management unit
DMAC unit
Stream processing unit
Device IF unit
30
32
33
34
35
36
AV IO block
Graphics engine unit
Video input format conversion unit
Imaging processing engine unit
Audio IF unit
Video output format conversion unit
41
42
43
44
45
40
Ain
Aout
Vin
Vout
108
LCD
107
Memory scheduler
Subsystem IF
Subsystem IF
Subsystem IF
Built-in RAM unit
Buffer unit
51
50
51a
51b
51c
52
53
73a
73b
72a
72b
74
71
60
70
High-speed IF 105
SDRAM (compatible for mobile communication)
106
104
Memory card
103
Another CPU
102
External bus
Flash memory unit
101

FIG. 14

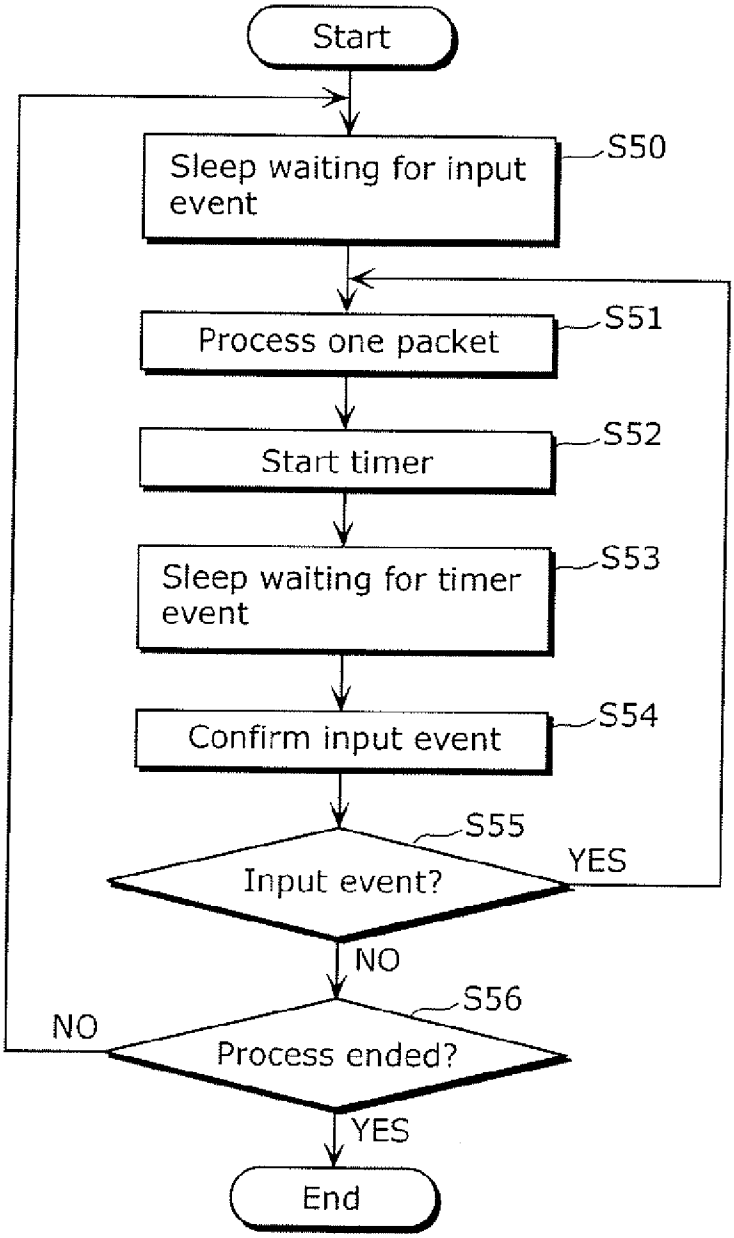

Start
Sleep waiting for input event
S50
Process one packet
S51
Start timer
S52
Sleep waiting for timer event
S53
Confirm input event
S54
Input event?
S55
YES
NO
Process ended?
S56
NO
YES
End

FIG. 15(a)

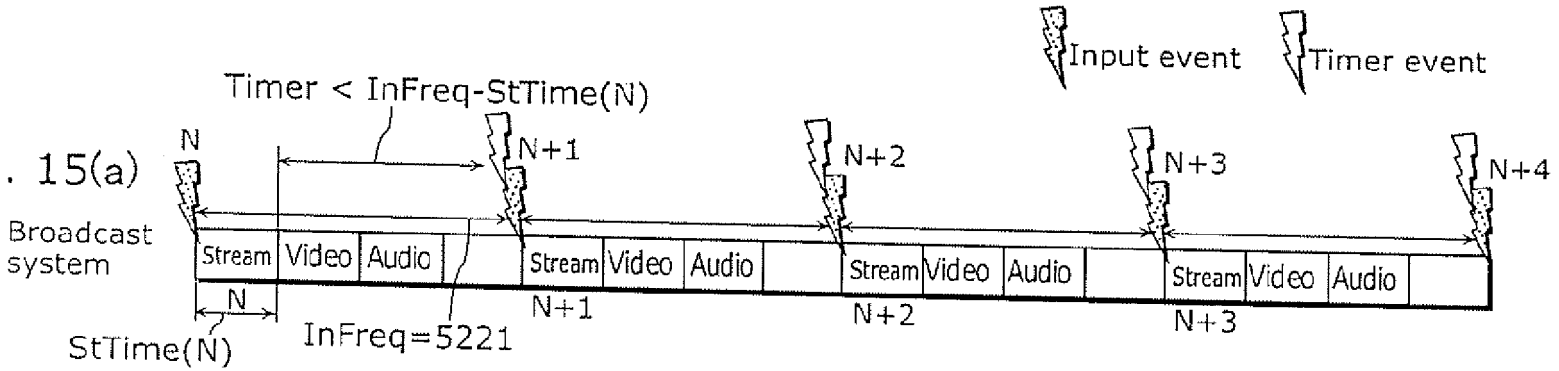
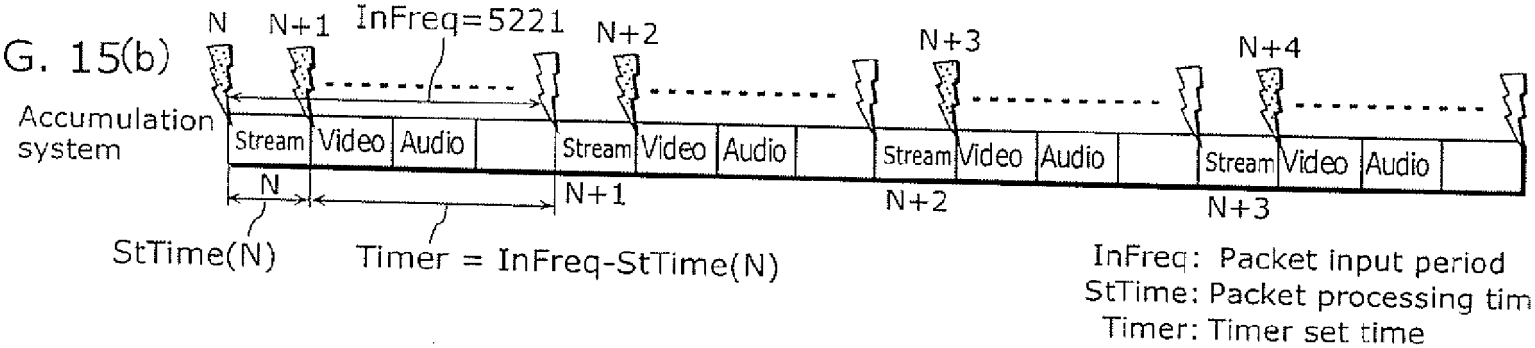


FIG. 15(b)



InFreq: Packet input period
StTime: Packet processing time
Timer: Timer set time

FIG. 16(a)

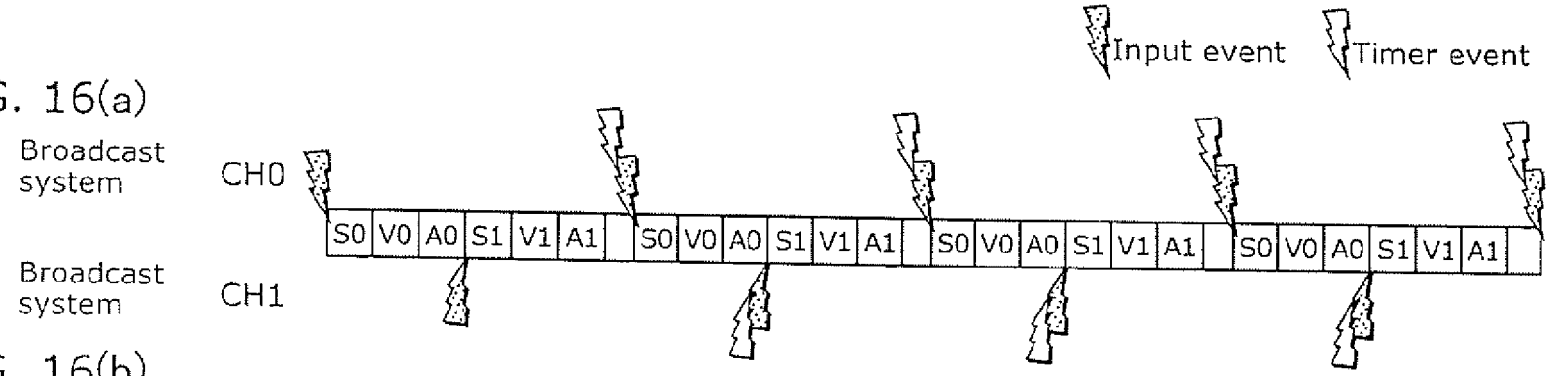


FIG. 16(b)

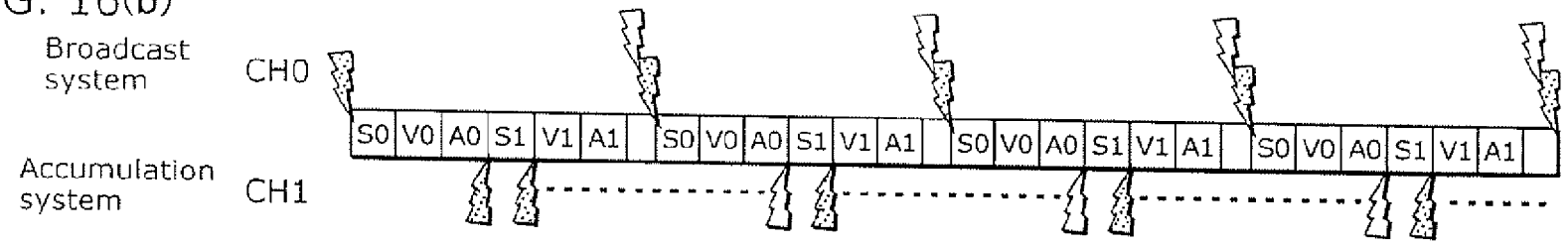
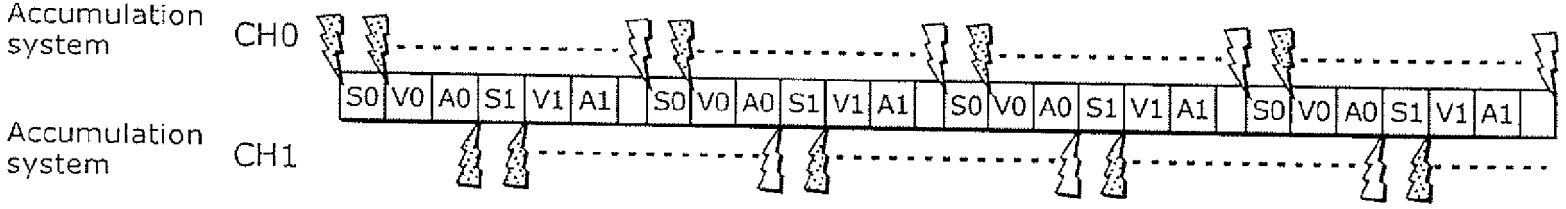



FIG. 16(c)